AMENDMENTS TO THE CLAIMS

Please amend claims 18 and 19 as set forth below:

1. (original) A content addressable memory (CAM) device comprising:
first and second rows of CAM cells;
a first pair of match lines coupled to the first row of CAM cells;
a second pair of match lines coupled to the second row of CAM cells; and
a first logic circuit coupled to a first match line of the first pair of match lines and to a first match line of the second pair of match lines, the first logic circuit being configured to output a match signal in a first state if both the first match lines indicate a match condition, and to output the match signal in a second state if either of the first match lines indicates a mismatch condition.

2. (original) The CAM device of claim 1 further comprising:
a first priority encoder coupled to the first match line of the first pair of match lines and to the second match line of the second pair of match lines; and
a second priority encoder coupled to the second match line of the first pair of match lines and to the first match line of the second pair of match lines.

3. (original)The CAM device of claim 2 wherein the first priority encoder is also coupled to receive the match signal output from the first logic circuit.

4. (original) The CAM device of claim 1 further comprising a select circuit to output either a match signal present on the first match line of the first pair of match lines or the match signal output from the first logic circuit, depending on the state of a first select signal.

5. (original) The CAM device of claim 4 further comprising:
an interface to receive an instruction; and
an control circuit coupled to receive the instruction from the interface and
configured to output the first select signal in either a first logic state or a second logic state according to the instruction.

6. (original) The CAM device of claim 5 wherein the control circuit is configured to generate the first select signal in a first state if the instruction indicates a single-word compare operation and in a second state if the compare instruction indicates a multiple-word comparand compare operation.

7. (original) The CAM device of claim 4 further comprising a configuration circuit to store a mode value and configured to output the first select signal in either a first logic state or a second logic state according to the mode value.

8. (original) The CAM device of claim 1 wherein each of the CAM cells within the first row of CAM cells comprises:
a storage circuit; and
first and second compare circuits coupled to the storage circuit.

9. (original) The CAM device of claim 8 wherein the first match line of the first pair of match lines is coupled to the first compare circuit of each of the CAM cells within the first row of CAM cells, and wherein the second match line of the first pair of match lines is coupled to the second compare circuit of each of the CAM cells within the first row of CAM cells.

10. (original) The CAM device of claim 1 further comprising a second logic circuit coupled to the second match line of the first pair of match lines and to the second match line of the second pair of match lines, the second logic circuit being configured to output a match signal in the first state if both the second match lines indicate a match condition, and to output the match signal in the second state if either of the second match lines indicates a mismatch condition.

11. (original) The CAM device of claim 10 further comprising a select circuit coupled to receive the match signal generated by the first logic circuit and the match signal generated by the second logic circuit, the select circuit being responsive to a select signal to output either the match signal generated by the first logic circuit or the match signal generated by the second logic circuit.

12. (original) The CAM device of claim 11 further comprising a configuration circuit to store a mode value and to output the select signal in either a first logic state or a second logic state according to the mode value.

13. (original) The CAM device of claim 11 further comprising:
an interface to receive a compare instruction; and
a control circuit coupled to receive the instruction from the interface and configured to output the select signal in either a first logic state or a second logic state according to the compare instruction.

14. (original) The CAM device of claim 1 further comprising a storage circuit coupled to the first match line of the first pair of match lines to store a match value

indicative of the state of the first match line of the first pair of match lines.

15. (original) The CAM device of claim 14 further comprising a logic AND gate coupled to receive the match value from the storage circuit and coupled to the first match line of the second pair of match lines.

16. (original) The CAM device of claim 1 wherein the first logic circuit comprises an AND gate having a first input coupled to the first match line of the first pair of match lines and a second input coupled to the first match line of the second pair of match lines.

17. (original) The CAM device of claim 16 further comprising storage circuits coupled to the first match lines to store the states of respective match signals thereon and to output the stored states of the respective match signals to the first and second inputs of the AND gate.

18. (currently amended) The CAM device of claim 1 further comprising:

a first pair of precharge circuits coupled respectively to the first match lines of the first pair of match lines and to the second match line of the second pairs of match lines; and

a second pair of precharge circuits coupled respectively to the second match lines of the first pair of match lines and to the first match line of the second pairs of match lines.

19. (currently amended) The CAM device of claim 18 further comprising circuitry to assert a first precharge enable signal to enable the first pair of precharge circuits to

precharge the first match lines of the first pair of match lines and the second match line of the second pair of match lines during a first interval, and to assert a second precharge enable signal to enable the second pair of precharge circuits to precharge the second match lines of the first pair of match lines and the first match line of the second pair of match lines during a second interval.

20. (original) The CAM device of claim 19 wherein the CAM device further comprises control circuitry to initiate a first compare operation in the first and second rows of CAM cells during the first interval and to initiate a second compare operation in the first and second rows of CAM cells during the second interval, the first compare operation producing match results on the second pair of match lines and the second compare operation producing match results on the first pair of match lines.

21. (original) A content addressable memory (CAM) device comprising:

a plurality of row pairs of CAM cells, wherein each row of CAM cells in a row pair is coupled to a plurality of match lines; and

a plurality of logic circuits each having inputs coupled to the plurality of match lines of a corresponding row pair of CAM cells, each of the plurality of logic circuits configured to selectively combine match results on the plurality of match lines of both rows of a corresponding row pair and output a composite match signal.

22. (original) The CAM device of claim 21 wherein each CAM cell within each row of CAM cells in a row pair includes a plurality of compare circuits coupled respectively to the plurality of match lines.

23. (original) The CAM device of claim 22 wherein each CAM cell within each row of CAM cells in a row pair includes a memory cell coupled to each of the plurality of compare circuits within the CAM cell.

24. (original) The CAM device of claim 21 wherein each of the plurality of logic circuits comprises a logic AND gate to logically AND the match results on a respective pair of match lines of the plurality of match lines.

25. (original) A content addressable memory (CAM) device comprising:

a plurality of CAM cells each including a first compare circuit and a second compare circuit;

a plurality of first match lines coupled to the first compare circuits included in the plurality of CAM cells;

a plurality of second match lines coupled to the second compare circuits included in the plurality of CAM cells; and

a plurality of logic circuits each coupled to a respective one of the first match lines and a respective one of the second match lines, each logic circuit being configured to output a match signal having a state according to the state of the one of the first match lines and the state of the one of the second match lines.

26. (original) The CAM device of claim 25 wherein each of the plurality of logic circuits is configured to output a match signal in a first state if the one of the first match lines indicates a match and the one of the second match lines indicates a match, each of the plurality of logic circuits being further configured to output a

match signal having a second state if either of the one of the first match lines and the one of the second match lines indicates a mismatch.

27. (original) The CAM device of claim 26 wherein each of the plurality of logic circuits comprises a logic AND gate having a first input coupled to the one of the first match lines and a second input coupled to the one of the second match lines.

28. (original) The CAM device of claim 27 wherein each of the plurality of logic circuits further comprises a select circuit having a first input coupled to an output of the logic AND gate and a second input coupled to the one of the first match lines.

29. (original) The CAM device of claim 28 wherein the select circuit is a multiplexer.

30. (original) The CAM device of claim 25 further comprising a priority encoder coupled to receive the match signals output by the plurality of logic circuits.

31. (original) A method of operation within a content addressable memory (CAM) device, the method comprising:
simultaneously performing first and second compare operations in an array of CAM cells to generate first and second sets of match signals; and
logically combining the first set of match signals with the second set of match signals to generate a set of resultant match signals.

32. (original) The method of claim 31 wherein simultaneously performing first and second compare operations in an array of CAM cells comprises simultaneously providing first and second comparands to the array of CAM cells via first and

second compare ports, respectively.

33. (original) The method of claim 32 wherein the CAM cells in the array of CAM cells are arranged in rows, each row of CAM cells being coupled to a corresponding pair of match lines, and wherein simultaneously performing first and second compare operations in the array of CAM cells further comprises receiving the first and second comparands in each of the rows of CAM cells, each row of CAM cells outputting a first match signal on a first match line of the corresponding pair of match lines according to whether the first comparand matches a value stored within the row of CAM cells, and each row of CAM cells outputting a second match signal on a second match line of the corresponding pair of match lines according to whether the second comparand matches the value stored within the row of CAM cells.

34. (original) The method of claim 31 wherein simultaneously performing first and second compare operations comprises simultaneously comparing a value stored within each CAM cell of the CAM array with a portion of a first comparand value and a portion of a second comparand value.

35. (original) The method of claim 31 wherein logically combining the first set of match signals with the second set of match signals comprises combining each match signal of the first set of match signals with a respective match signal of the second set of match signals to generate a respective one of the resultant match signals.

36. (original) The method of claim 35 wherein combining each match signal of the first set of match signals with a respective match signal of the second set of match signals comprises logically ANDing each match signal of the first set of match signals with the respective match signal of the second set of match signals to generate the respective one of the resultant match signals.

37. (original) The method of claim 31 further comprising selecting either the set of resultant match signals or the first set of match signals to be output as a selected set of match signals.

38. (original) The method of claim 37 further comprising generating a match address based on the selected set of match signals.

39. (original) A content addressable memory (CAM) device comprising:
an array of CAM cells;
means for simultaneously performing first and second compare operations in the array of CAM cells to generate first and second sets of match signals; and
means for logically combining the first set of match signals with the second set of match signals to generate a set of resultant match signals.

40. (original) The CAM device of claim 39 wherein the means for simultaneously performing first and second compare operations in the array of CAM cells comprises means for simultaneously providing first and second comparands to the array of CAM cells via first and second compare ports, respectively.

41. (original) The CAM device of claim 39 wherein the means for simultaneously performing first and second compare operations comprises means for simultaneously comparing a value stored within each CAM cell of the CAM array with a portion of a first comparand value and a portion of a second comparand value.

42. (original) The CAM device of claim 39 wherein the means for logically combining the first set of match signals with the second set of match signals comprises means for combining each match signal of the first set of match signals with a respective match signal of the second set of match signals to generate a respective one of the resultant match signals.

43. (original) The CAM device of claim 39 further comprising means for selecting either the set of resultant match signals or the first set of match signals to be output as a selected set of match signals.

44. (original) The CAM device of claim 43 further comprising means for generating a match address based on the selected set of match signals.